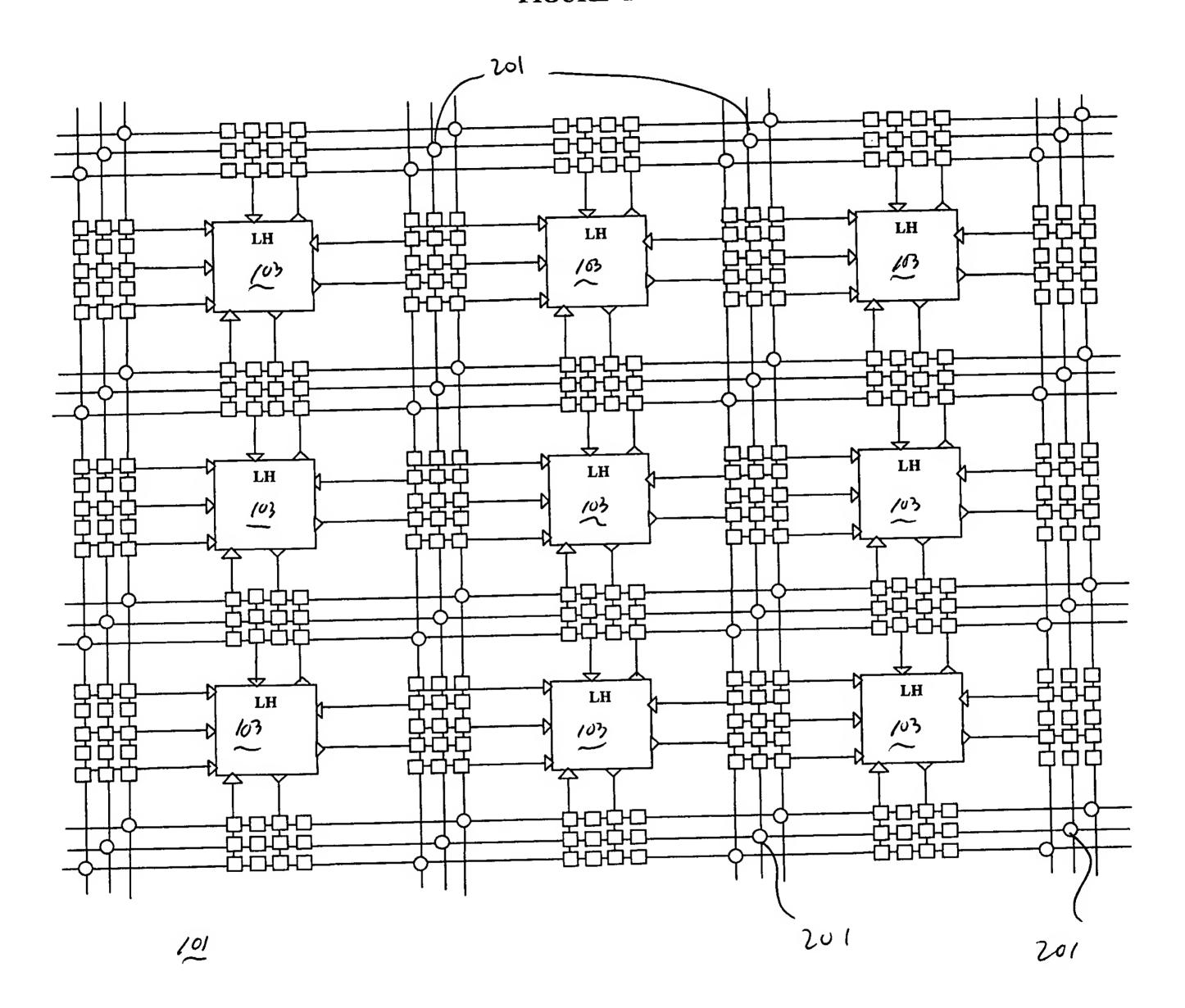
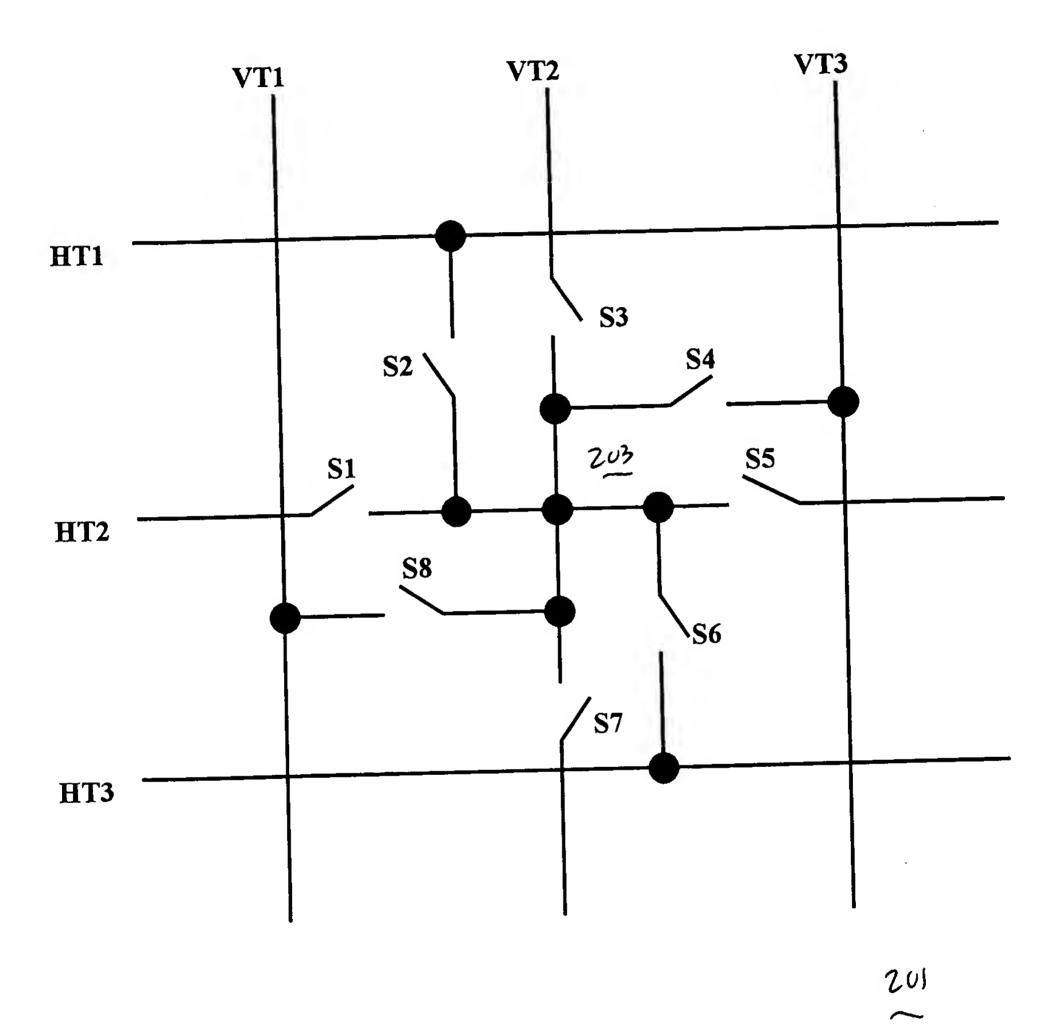
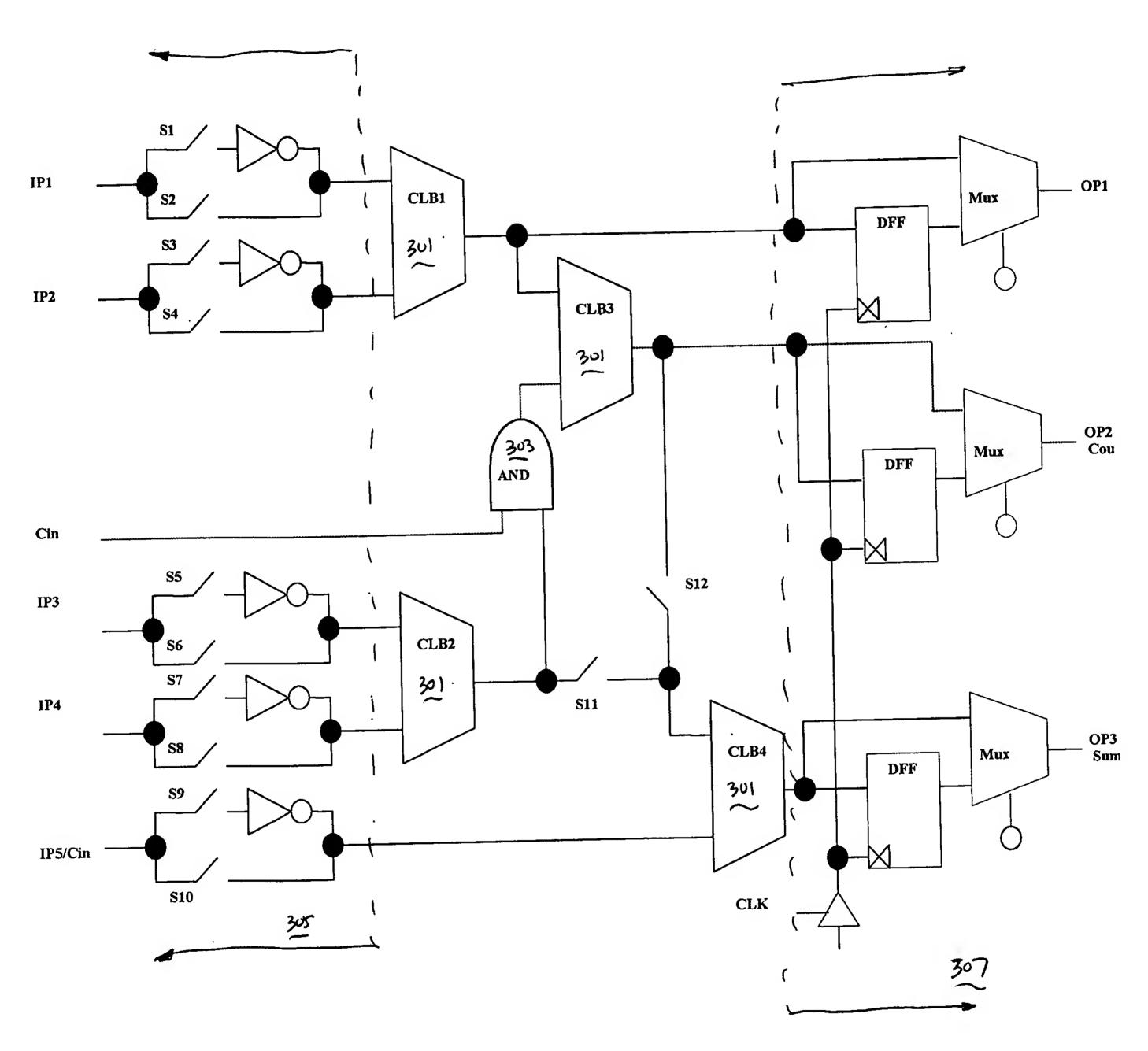
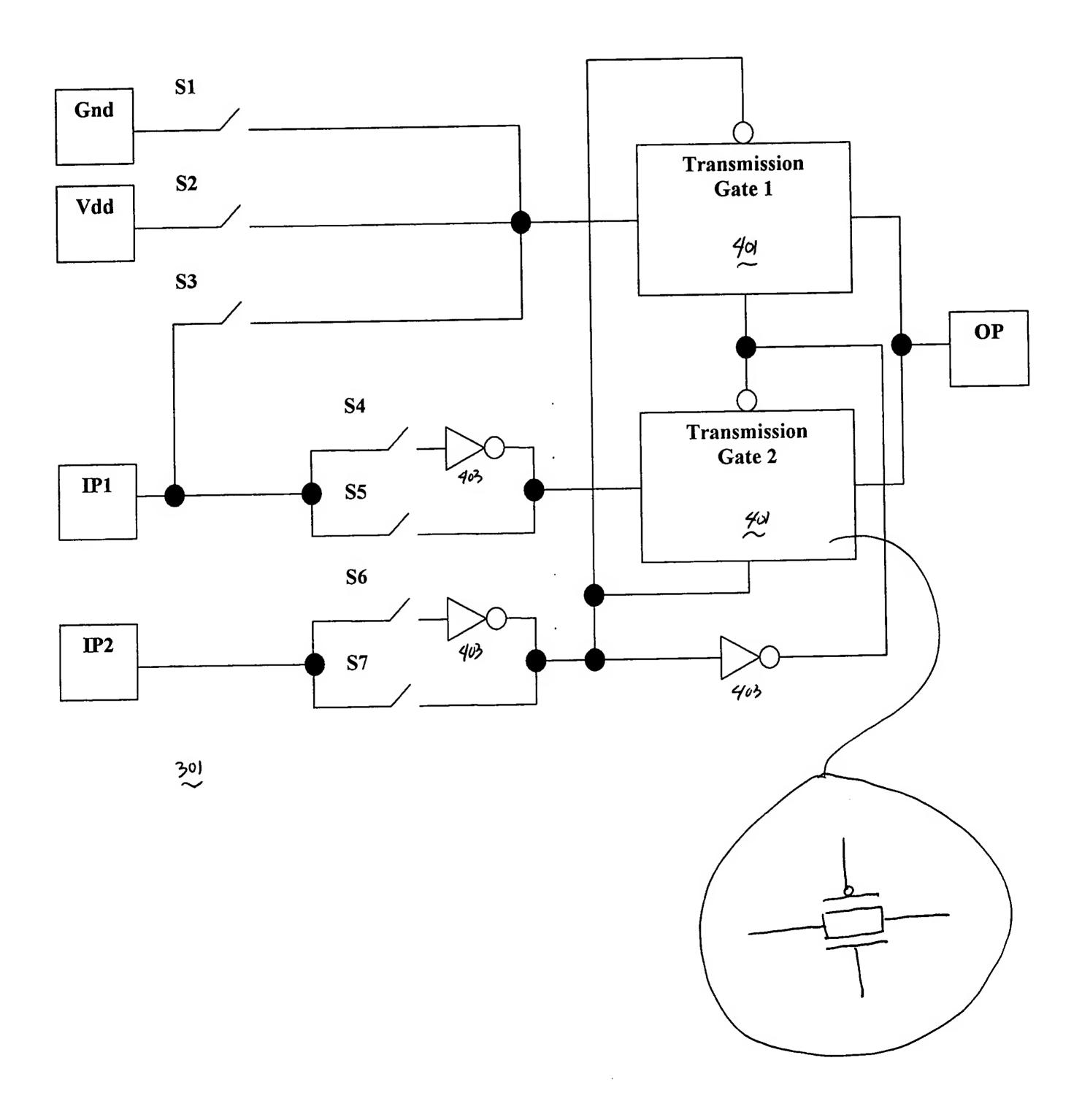
FIGURE 1

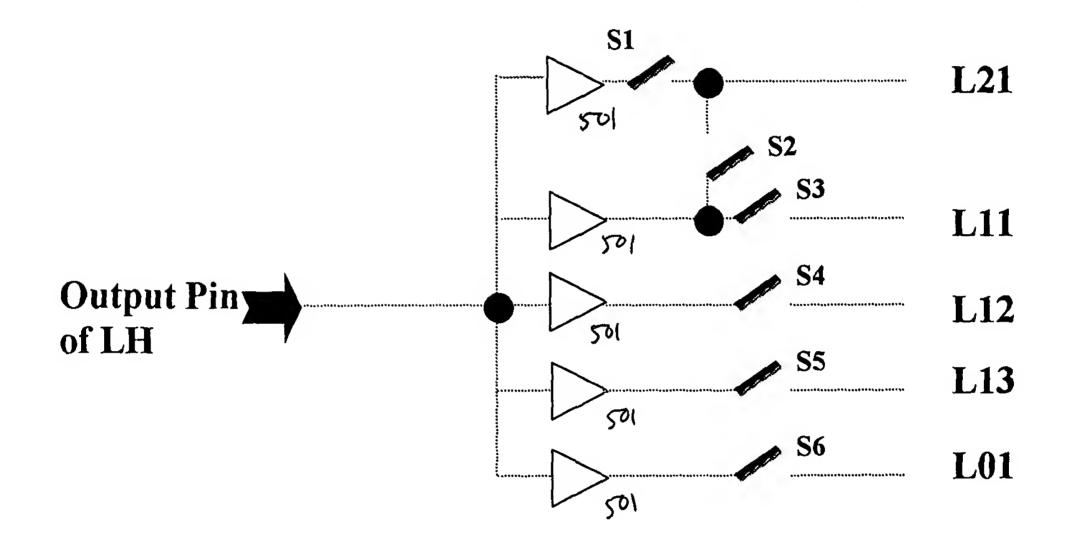


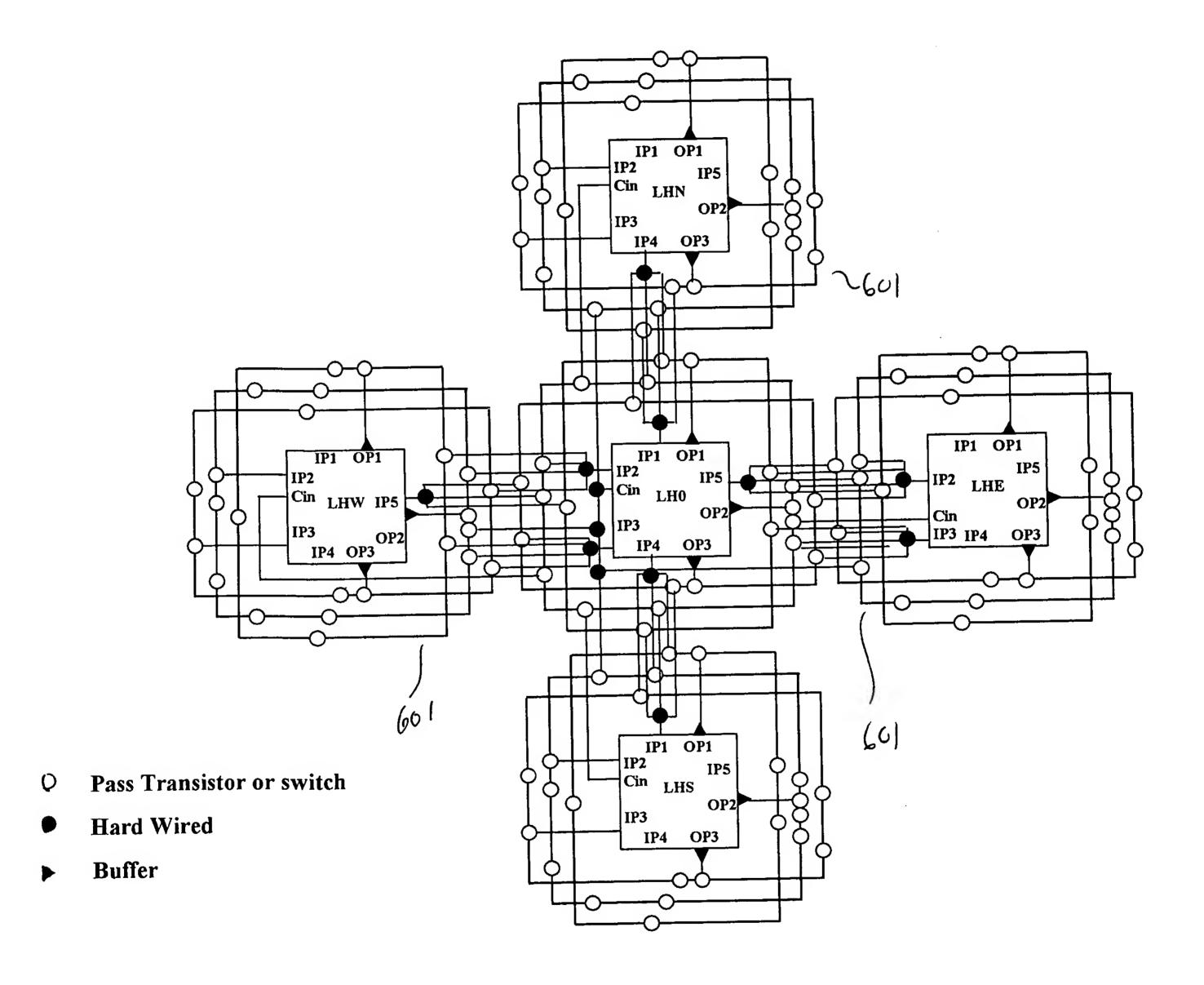




CLB: Cascadable Logic Block







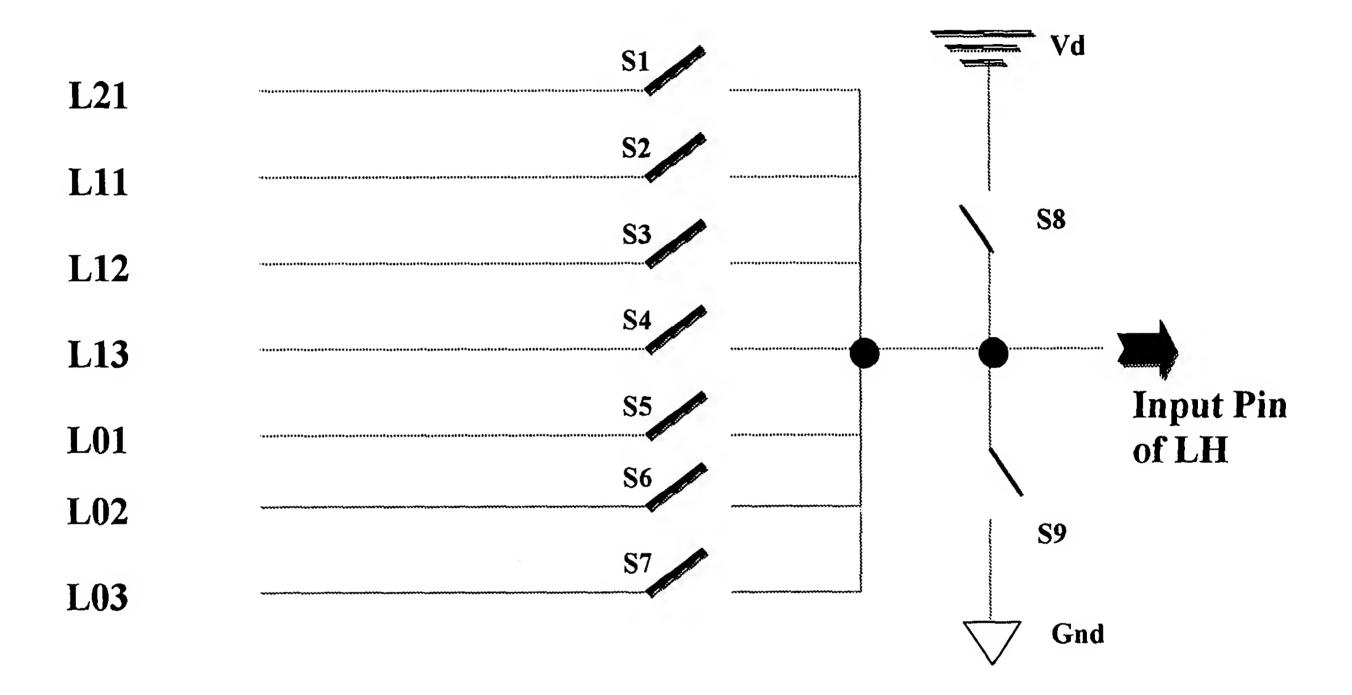


FIGURE 8

LH	LH	LH	LH	LH	LH	LH	LH	LH	
LH	LH	LH	LH	LH	LH	LH	LH	LH	
LH	LH	LH	LH	LH	LH	LH	LH	LH	ŀ
LH	LH	LH	LH	LH	LH	LH	LH	LH	501
LH	LH	LH	LH	LH	LH	LH	LH	LH	
LH	LH	LH	LH	LH	LH	LH	LH	LH	
LH	LH	LH	LH	LH	LH	LH	LH	LH	
LH	LH	LH	LH	LH	LH	LH	LH	LH	
LH	LH	LH	LH	LH	LH	LH	LH	LH	
LH	LH	LH	LH	LH	LH	LH	LH	LH	
1 ————————————————————————————————————		801		LJ	,	<u></u>	<u> </u>	1	

FIGURE 9

SWITCH	S1	S2	S3	S4	S5	S6	S7	Equation
AND2		X	X	X		X		OP = IP1 & IP2
NAND2	X		X		X	X		OP = ! (IP1 & IP2)
OR2	X		X	X	\ \ \	<u></u>	X	OP = IP1 IP2
NOR2		X	X		X	V	X	OP = ! (IP1 IP2)
XOR2	X	X			X	X		OP = (IP1 & !IP2) (!IP1 & IP2)
XNOR2	X	X			X		X	OP = (IP1 & IP2) (!IP1 & !IP2)

Notes: \checkmark : Switch on >>: Switch off

FIGURE 10

